REMARKS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1, 6-14, and 21-26 are pending in this case. Claims 1 and 11 are amended herein and claims 2-5 and 15-20 are cancelled herein. Claims 21-26 are added herein.

The Examiner objected to claims 7, 8, and 14 in that they should depend from claim 2. Applicant believes the amendments to claim 1 overcome this objection.

The Examiner rejected claims 1, 2, 6, 9, 10 and 14-17 under 35 U.S.C. 102(e) as being anticipated by Buynoski (U.S. Patent 6,583,012).

Applicant respectfully submits that amended claim 1 is unanticipated by Buynoski as there is no disclosure or suggestion in the reference of etching the mold layer to create a second opening after depositing the first metal and depositing a second metal in the second opening to form a second metal gate electrode. Instead, Buynoski teaches simultaneously forming two openings in an insulative layer and depositing the same metal in both openings. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are unanticipated by Buynoski.

The Examiner rejected claims 3, 7, 11, 12 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Buynoski (U.S. Patent 6,583,012) in view of Takeuchi (U.S. 2004/0080001).

Claim 3 is cancelled and its limitations have been incorporated into claim 1.

Applicant respectfully submits that amended claim 1 is patentable over Buynoski in view of Takeuchi as there is no disclosure or suggestion in the references of etching the mold layer to create a second opening after depositing the first metal and depositing a second metal in the second opening to form a second metal gate electrode. Instead, Buynoski teaches simultaneously forming two openings in an insulative layer and depositing the same metal in both openings. Takeuchi teaches forming dummy gates 26, then forming insulating film 23, and then separately removing the dummy gate in the p-channel regions and the n-channel regions. There is no disclosure or suggestion in Takeuchi of, after depositing the first metal, etching the mold layer to form a second opening. Instead of etching a mold layer, Takeuchi removes the dummy gate. A proper combination of the references would not accomplish the claimed invention.

The problems associated forming a polysilicon (dummy) gate and its replacement are discussed in the background of the instant application in paragraphs [0007]-[0011], the "gate-last fabrication scheme." The claimed invention overcomes these problems in that the (second) opening is formed by etching the mold layer rather than removing a dummy gate as in Takeuchi. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are patentable over Buynoski in view of Takeuchi.

The Examiner rejected claims 4, 5 and 8 under 35 U.S.C.§ 103(a) as being unpatentable over Buynoski (U.S. Patent 6,583,012) in view of Takeuchi (U.S. 2004/0080001) as applied to claims 2 and 3 above, and further in view of Liang (U.S. Patent 6,130,123).

Claims 4 and 5 are cancelled due to inconsistencies with the amendment to claim 1.

Applicant respectfully submits that claim 8 is patentable over Buynoski in view of Takeuchi and Liang as there is no disclosure or suggestion in the references of etching the mold layer to create a second opening after depositing the first metal and depositing

a second metal in the second opening to form a second metal gate electrode, as required by claim 1 from which claim 8 depends. The combination of Buynoski and Takeuchi does not disclose or suggest this feature. Liang is added by the Examiner to teach the first metal work function between 4 and 4.2 and a second metal work function between 5 and 5.2. Accordingly, Applicant respectfully submits that claim 8 is patentable over the references.

Applicant respectfully submits that new claim 21 is patentable over the references as there is no disclosure or suggestion in the references of etching a first mold layer to create a first opening, creating a first metal gate electrode, removing the first mold layer, forming a second mold layer, then, etching the second mold layer to create a second opening, and depositing a second metal in the second opening. As discussed above, the combination of Buynoski and Takeuchi fails to teach etching a mold layer to create a second opening after creating the first metal gate electrode. Furthermore, the combination of Buynoski and Takeuchi fails to teach a second mold layer and etching the second mold layer to create a second opening. Liang fails to teach mold layers at all. Accordingly, there is no disclosure or suggestion in the references creating a first metal gate electrode, forming a second mold layer and then etching the second mold layer to create a second opening.

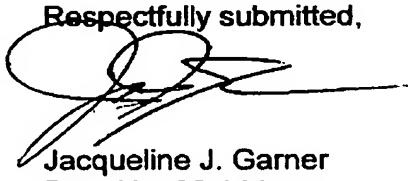
The Examiner applies Liang to teach that "the simple method of depositing complementary metals one after the other will damage the thin gate dielectric during patterning . . . ." Applicant agrees. However, the Examiner then argues that this teaching somehow suggests that a second metal could be used "if a second mold layer of different composition is deposited (to alter the etching characteristic of the mold material) and an opening is made for depositing the second gate metal . . . ." There is no suggestion in Liang for using a mold layer and there is no suggestion in Liang of

using a different composition to alter an etching characteristic to avoid gate dielectric damage. Liang merely notes that damage occurs and provides a non-etching approach to solve the problem. There is nothing in Liang that when combined with the teachings of Buynoski and Takeuchi would accomplish the claimed invention. Accordingly, Applicant respectfully submits that claim 21 and the claims dependent thereon are patentable over the references.

The other references cited by the Examiner have been reviewed, but are not felt to come within the scope of the claims as amended.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1, 6-14, and 21-26. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,



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